REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on April 27, 2001, and the references cited therewith. Furthermore, Applicants formally traverse herewith all rejections presented therein.

Claims 1, 7, and 14 have been amended consistent with the originally filed specification. Accordingly, entry of these amendments is believed to be in order and is not believed to introduce any new matter. By way of example only, the Examiner's attention is directed to the originally filed specification, page 12.

§102 Rejection of the Claims

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 102(a) as being anticipated by, or in the alternative, under 35 USC § 103(a) as obvious over Horiguchi et al. ("A Direct Tunneling Memory (DTM) Utilizing Novel Floating Gate Structure"). However, Horiguchi lacks each an every element of Applicants' amended claims 1, 7, and 14.

More specifically, Applicants amended claims require edge-defined vertical gates. As will be readily appreciated by those skilled in the art, edge-defined MOS technology ("EDMOS") permits sub-lithographic dimensions of gate lengths and widths. Furthermore, unlike standard lithographically defined geometrics, EDMOS uses the thickness of the deposited films in determining gate lengths and widths.

Horiguchi is directed to a floating gate memory having Direct Tunneling Memory, wherein an ultra-thin tunnel oxide, with leakage stop barrier and sidewall control gate, prevents the overlap between a floating gate and source/drain extensions, thereby suppressing gate leakage current and improving retention time while high speed operations with low voltage are achieved.

Yet, Horiguchi very specifically indicates that standard lithography is used in the manufacturing process. Accordingly, Horiguchi fails to disclose or teach, either expressly or inherently, all the required elements of Applicants' amended independent claims 1, 7, and 14 since edge-defined vertical gates are not present and correspondingly sub-lithographic dimensions are not achieved. Therefore, Applicants respectfully request that the rejection of independent claims 1, 7, and 14 be withdrawn.

Further, claims 2-6, 8-13, and 15-22 are dependent claims derived from the rejected independent claims 1, 7, and 14, respectively. Correspondingly, the rejection of these claims is no longer sustainable, and the Applicants respectfully request that these rejections be withdrawn.

Claims 1-11, 13-17, and 19-23 were rejected under 35 USC § 102(e) as being anticipated by, or in the alternative, under 35 USC § 103(a) as obvious over Lin et al. (U.S. Patent No. 6,078,076).

Lin is directed to vertical channels in split-gate flash memory cells. Lin fails to disclose or teach either expressly or inherently, edge-defined vertical gates as is required by Applicants' amended independent claims 1, 7, and 14. In fact, Lin does not achieve sub-lithographic dimensions. (Lin, col. 7, lines 13-28). Accordingly, the rejection of claims 1-11, 13-17, and 21-23 must be withdrawn and Applicants respectfully request an indication of the same.

Claims 1-10, 13-15, 17, 19, and 21-23 were rejected under 35 USC § 102(e) as being anticipated by, or in the alternative, under 35 USC § 103(a) as obvious over Yang (U.S. Patent No. 6,093,945).

Yang is directed to a split gate flash memory with minimum over-erase problem. However, Yang uses conventional photolithography, cannot achieve sub-lithographic dimensions, and does not disclose or teach, either expressly or inherently, edge-defined vertical gates. (E.g., Yang, col. 3, lines 43-48; col. 8, lines 29-36) Therefore, Applicants respectfully request that the rejection of claims 1-10, 13-15, 17, 19, and 21-23 be withdrawn.

§103 Rejection of the Claims

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213).

Watanabe is directed to a non-volatile semiconductor memory device with inter-layer insulation film. Watanabe does not disclose or teach, either expressly or inherently, edge-defined vertical gates as required by Applicants' amended independent claims 1, 7, and 14. More specifically, Watanabe's gate dimensions are determined by lithographically defined geometrics. In fact, standard photolithographic technique is used in Watanabe. (E.g., Watanabe,

col. 2, lines 34-36; col. 9, lines 8-14; col. 11, lines 16-21 and 43-48) Correspondingly, sub-lithographic gate dimensions are not achieved.

Hong is directed to a top floating-gate flash EEPROM structure. Hong does not disclose or teach, either expressly of inherently, edge-defined vertical gates as required by Applicants' amended independent claims 1, 7, and 14. Moreover, Hong uses conventional lithography and does not achieve sub-lithographic dimensions. (E.g., Hong, col. 3, lines 52-54; col. 4, lines 29-34)

It is fundamental that in order to sustain an obviousness rejection, each and every required element must be shown to exist, either expressly or inherently in the cited references. However, as presented above, none of the relied upon references standing alone or in combination, teach or disclose, either expressly or inherently an edge-defined vertical gate. Accordingly, the Applicants respectfully request that the rejection of claims 1-23 be withdrawn.

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,078,076) in view of Watanabe (U.S. Patent No. 6,133,601) or Hong et al. (U.S. Patent No. 5,625,213).

As presented above, Lin, Watanabe, and Hong, standing alone or in combination with one another, fail to disclose or teach, either expressly or inherently an edge-defined vertical gate. Correspondingly, the rejections of claims 1-23 cannot be sustained and Applicants respectfully request that the rejection be withdrawn.

Claim 17 was rejected under 35 USC § 103(a) as being unpatentable over Lin et al. (U.S. Patent No. 6,078,076) or Horiguchi in view of Yang (U.S. Patent No. 6,093,945).

Again, as discussed above, neither Lin nor Horiguchi, alone or in combination, teaches or discloses, either expressly or inherently an edge-defined vertical gate as required by each of Applicants' amended independent claims 1, 7, and 14. Therefore, the rejection of claim 17 should be withdrawn, and the Applicants respectfully request the same.

Claims 1-23 were rejected under 35 USC § 103(a) as being unpatentable over Watanabe (U.S. Patent No. 6,133,601) in view of Hong et al. (U.S. Patent No. 5,625,213), Lin et al. (U.S. Patent No. 6,078,076), or Yang (U.S. Patent No. 6,093,945).

As has been presented in detail above, a rejection based on obviousness can no longer be sustained, since none of the cited references teach or disclose, either expressly or inherently an

edge-defined vertical gate, as is required by Applicants' amended independent claims 1, 7, and 14. Accordingly, Applicants respectfully request that the rejection of claims 1-23 be withdrawn.

CONCLUSION

Applicants sincerely believe that the above amendment and response represents a complete response to each and every rejection presented by the Examiner.

Furthermore, the Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney, Joseph Mehrle, at (612) 373-6975 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 27 day of August, 2001.

Name Tina Pugh

Signature _____